GAU 2133
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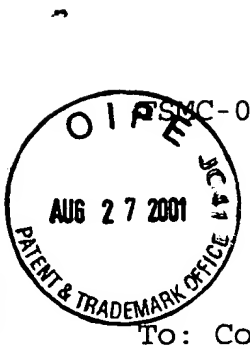

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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
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Subject: Serial No. 09/883,449 06/18/01

Nai-Yin Sung, Ming-Chyuan Chen

A METHOD TO VERIFY THE PERFORMANCE OF BIST CIRCUITRY FOR TESTING EMBEDDED MEMORY

Grp. Art Unit: 2133

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,012,157 to Lu, "System for Verifying the Effectiveness of a RAM BIST Controller's Ability to Detect Faults in a RAM Memory Using States Indicating by Fault Severity Information," teaches a system to evaluate the effectiveness of a BIST controller by simulation.

U.S. Patent 5,822,228 to Irrinki et al., "Method for Using Built in Self Test to Characterize Input-to-Output Delay Time of Embedded Cores and Other Integrated Circuits," discloses a method for measuring propagation delays of embedded cores and of integrated circuits.

U.S. Patent 5,513,339 to Agrawal et al., "Concurrent Fault Simulation of Circuits with Both Logic Elements and Functional Circuits," teaches a method to simulate a circuit containing both logic gates and memory blocks to determine fault detection.

U.S. Patent 5,475,624 to West, "Test Generation by Environment Emulation," discloses a method to aid development of fault detection test patterns using emulators.

J. Dreibelbis, et al., "Processor-Based Built-In Self-Test for Embedded DRAM", IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, November 1998, pp. 1731-1740, teaches a BIST circuit wherein additional flexibilty is achieved through the use of processor elements, such as an instruction counter, a instruction memory, and a branch controller.

"Built-In Self-Test (BIST) Using Boundary Scan", Texas Instruments Corp., Dec. 1996, pp. 1-8, discloses a boundary scan test architecture that supports BIST.

I. Burgess, "Test and Diagnosis of Embedded Memory Using BIST," Mentor Graphics Corp., Sept. 2000, pp. 1-6, teaches an augmentation to a BIST controller to enable a scan out of failed memory data to aid in diagnosis.

Sincerely,

George O. Saile,
Reg. No. 19572